AMENDMENTS TO THE CLAIMS

Claims 1-6 (Cancelled)

7. (Previously presented) The method of claim 37, wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame.

8. (Previously presented) The method of claim 37, wherein the nodes transmit a plurality of messages in each of a plurality of frames on the first line of the serial data bus, the first message is at least one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once each minor frame.

9. (Previously presented) The method of claim 37, wherein determining whether the first message was received includes waiting for a reply from the second node.

10. (Previously presented) The method of claim 37, further comprising:

detecting a current surge in a bus interface circuit operatively connecting the second node to the first bus; and

cycling power to the bus interface circuit in response to detecting the current surge in the bus interface circuit.

11. (Previously presented) The method of claim 37, wherein the second bus is a different type of bus than the serial data bus.

Claims 12-14 (Cancelled)

15. (Previously presented) The system of claim 41, wherein the nodes further detect a current surge in the bus interface and report the current surge in the bus interface circuit to the node sending the first message.

16. (Previously presented) The system of claim 41, wherein the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame.

17. (Previously presented) The system of claim 41, wherein the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once in each minor frame.

18. (Previously presented) The system of claim 41, wherein each node includes a bus interface circuit operatively connected to the serial data bus; means for detecting a current surge in the bus interface circuit; and means for cycling power to the bus interface circuit in response to detecting the current surge.

19. (Previously presented) The system of claim 41, wherein the second bus is a different type of bus than the first bus.

20. (Previously presented) The system of claim 41, wherein the nodes include a bus interface circuit operatively connected to the serial data bus; and means for receiving the recovery command on the second bus and for re-initializing the bus interface circuit in response to the recovery command.

Claims 21-36 (Cancelled)

37. (Currently amended) A method of clearing latch-up and other single event functional interrupts in a data processing system having a plurality of nodes operatively connected to a serial data bus, the method comprising:

periodically transmitting a first message from a first node to a second node on a first line of the serial data bus;

determining whether the first message was received by the second node; and

transmitting a recovery command to the second node if the second node does not respond to the first message, the recovery command transmitted via ~~a second line of the serial bus or by another~~ an alternative data bus path, the recovery command causing the second node to disrupt a monostable condition in the second node and restore functionality of the second node without disrupting the first node and any other nodes of the plurality.

38. (Previously presented) The method of claim 37, wherein the second node includes a physical layer controller connected to the serial data bus and link layer controller; and wherein a monostable condition is disrupted in at least one of the physical layer controller and the link layer controller.

39. (Previously presented) The method of claim 37, wherein the link layer controller is coupled to and dc-isolated from the physical layer controller; and wherein disrupting a monostable condition in the link layer controller is independent of disrupting a monostable condition in the physical layer controller.

40. (Previously presented) The method of claim 37, wherein the recovery command causes a bus interface circuit operatively connecting the second node to the first bus to be re-initialized.

41. (Currently amended) A data processing system comprising:

a serial data bus including at least one line; and

a plurality of nodes operatively connected to the serial data bus, each node including a bus interface connected to the serial data bus;

wherein at least one of the nodes periodically transmits a first message on a first line of the serial data bus to other nodes, and transmits a recovery command to a node that does not respond to the first message, the recovery command transmitted via a second line of the serial bus or by a second data bus; and

wherein [[a]] the non-responding node receives the recovery command and, in response, clears a latch-up and restores correct operation, including disrupting a monostable condition.

42. (Previously presented) The system of claim 41, wherein the bus interface includes a physical layer controller that is connected to the serial data bus, and a link layer controller that is coupled to and galvanically isolated from the physical layer controller, and wherein a monostable condition in the link layer controller is disrupted independently of a monostable condition in the physical layer controller.

43. (Previously presented) The system of claim 42, wherein each node further includes a second data bus and means for coupling the link layer controller to the second data bus, the means also dc-isolating the link layer controller from the second data bus.

44. (Currently amended) The system of claim 41, wherein each node further includes ~~nodes further include~~ a watchdog timer for monitoring its bus interface.

45. (Previously presented) The system of claim 41, wherein clearing the latch-up and restoring correct operation includes turning off and then turning back on the bus interface, and also reinitializing affected bus circuitry.

46. (Previously presented) The system of claim 41, wherein the bus interface is not radiation-hardened.